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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/638,026	08/14/2000	Paul A. Farrar	M4065.0082/P082-A	8833

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EXAMINER	
PAREKH, NITIN	

ART UNIT	PAPER NUMBER
2811	

DATE MAILED: 12/21/2004

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	09/638,026	FARRAR, PAUL A.	
	Examiner	Art Unit	
	Nitin Parekh	2811	

-- *The MAILING DATE of this communication appears on the cover sheet with the correspondence address* --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *25 October 2004*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *40,43-51,68-72 and 74-86* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☒ Claim(s) *76-86* is/are allowed.

6)☒ Claim(s) *40,43-51,68-72,74 and 75* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *08-14-2000* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☐ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Request for Continued Examination

1. A request for continued examination (RCE) under 37 CFR 1.114, including the fee set forth in 37 CFR 1.17(e), was filed in this application after final rejection. Since this application is eligible for continued examination under 37 CFR 1.114, and the fee set forth in 37 CFR 1.17(e) has been timely paid, the finality of the previous Office action has been withdrawn pursuant to 37 CFR 1.114. Applicant's submission filed on 10/25/04 has been entered. An action on the RCE follows.

2. The amendment filed on 10/25/2004 has been entered.

Claim Rejections - 35 USC § 103

3. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

4. Claims 40, 43-49, 68, 71, 72, 74 and 75 are rejected under 35 U.S.C. 103(a) as being unpatentable over Yamamoto (US Pat. 5925931) in view of Svetkoff et al. (US Pat. 6249347).

Regarding claim 40, Yamamoto discloses a semiconductor device/an integrated circuit (IC) chip on a semiconductor substrate/silicon wafer (21/22 in Fig. 7) comprising:

- a semiconductor structure having a metal contact (23 in Fig. 7) formed on the surface thereof
- a first insulator layer (24/41 in Fig. 7) overlying the metal contact
- a metal pad/interconnection (50 in Fig. 7) overlying the first insulator layer and in contact with the metal contact, the metal pad being partially overtop of the metal contact and comprising a stack of three different metals/levels including zinc or nickel, copper and gold (see 46A, 46B and 50 in Fig. 4 and 7; Col. 5, lines 9-35)
- a second insulator layer (47 in Fig. 7) overlying the metal pad
- the metal contact being connected to the metal pad by a via hole (25/42 in Fig. 7) in the first insulator, and
- solder contact/ball (48 in Fig. 7) formed in the second insulator layer and in contact with the metal pad, the solder contact/ball extending from the top of the second insulator layer to the metal pad by a through-hole formed in the second insulator (Fig. 7)

(Fig. 7; Col. 6, line 40- Col. 7, line 5; Col. 4-8).

Yamamoto fails to teach the diameter of the solder contact being less than 100 microns.

Svetkoff et al. teach a miniature/micro ball grid array (BGA) device using solder balls (200 in Fig. 11) having a typical range of 10-300 microns to achieve the increased

interconnect density and very fine geometries/ground rules (Col. 11, lines 27-37; Col. 1 and 2).

It would have been obvious to a person of ordinary skill in the art at the time invention was made to incorporate the solder contacts having diameter less than 100 microns as taught by Svetkoff et al. so that interconnect density can be improved and the device size/ground rules can be reduced in Yamamoto's device.

Regarding claims 43 and 44, Yamamoto and Svetkoff et al. teach substantially the entire claimed structure as applied to claim 40, except the solder contacts having the diameter of less than 10 microns or that being approximately 2 microns respectively.

The determination of parameters such as size/dimension, range and shape of the metal/solder contacts and metallization structure including diameter, pitch/spacing, pad dimension, number/thickness of an insulating layer, number/diameter of vias, etc. in chip packaging and interconnection technology art is a subject of routine experimentation and optimization to achieve the desired I/O density, line width/ground rules, performance and reliability.

It would have been obvious to a person of ordinary skill in the art at the time invention was made to incorporate the solder contacts having diameter less than 10 microns, approximately 2 microns or having a range of 2-100 microns as taught by Svetkoff et al. so that interconnect density can be improved and the device size/ground rules can be reduced in Yamamoto's device.

Regarding claim 45, Yamamoto and Svetkoff et al. teach substantially the entire claimed structure as applied to claim 40 above, wherein Yamamoto teach the metal contact being connected to the metal pad by a via hole (25/42 in Fig. 7) formed in the first insulator.

Regarding claim 46, Yamamoto and Svetkoff et al. teach substantially the entire claimed structure as applied to claim 40 above, wherein Yamamoto teach the solder contacts being extended from the top of the second insulator layer to the metal pad by a through-hole formed in the second insulator (see Fig. 7).

Regarding claim 47, Yamamoto and Svetkoff et al. teach substantially the entire claimed structure as applied to claim 40 above, wherein Yamamoto teach the metal pad being partially overtop of the metal contact (see Fig. 7).

Regarding claim 48, Yamamoto and Svetkoff et al. teach substantially the entire claimed structure as applied to claim 40 above, wherein Yamamoto teaches the semiconductor device being the IC chip (21/22 in Fig. 7).

Regarding claim 49, Yamamoto and Svetkoff et al. teach substantially the entire claimed structure as applied to claim 40 above, including the semiconductor device being an IC wafer (21/22 in Fig. 7).

Regarding claim 68, Yamamoto and Svetkoff et al. teach substantially the entire claimed structure as applied to claim 40 above, except the first insulating layer being 2 microns thicker than the metal contact.

Yamamoto further teaches the first insulating layer being 10-50 microns thick (41 in Fig. 7; Col. 4, line 39) and as shown in Fig. 7, the insulating layer being approximately 2-3 times thicker than the metal pad/contact (23 in Fig. 7) or more than 2 microns thicker than the metal pad/contact.

It would have been obvious to a person of ordinary skill in the art at the time invention was made to incorporate the solder contacts having diameter less than 100 microns as taught by Svetkoff et al. and the first insulating layer being 2 microns thicker than the metal contact so that the interconnect density and passivation/insulation integrity can be improved in Yamamoto's device.

Regarding claim 71, Yamamoto and Svetkoff et al. teach substantially the entire claimed structure as applied to claims 40 and 43 above, including the solder contacts having the diameter between 2-100 microns.

Regarding claim 72, Yamamoto and Svetkoff et al. teach substantially the entire claimed structure as applied to claims 40 and 43 above, including the solder contacts having the diameter of approximately 2 microns.

Regarding claim 74, Yamamoto and Svetkoff et al. teach substantially the entire claimed structure as applied to claims 40 and 43 above, including the solder contacts having the diameter of less than 50 microns.

Regarding claim 75, Yamamoto and Svetkoff et al. teach substantially the entire claimed structure as applied to claims 40 and 43 above, including the solder contacts having the diameter of less than 25 microns.

5. Claims 50 and 51 are rejected under 35 U.S.C. 103(a) as being unpatentable over Yamamoto (US Pat. 5925931) and Svetkoff et al. (US Pat. 6249347) as applied to claim 40 above, and further in view of the admitted prior art (APA).

Regarding claims 50 and 51, Yamamoto and Svetkoff et al. teach substantially the entire claimed structure as applied to claim 40 above, except the device being bonded to a module substrate or a circuit board respectively.

APA teaches a semiconductor device being bonded to a module substrate or a circuit board (specification page 2; Fig. 1-3).

It would have been obvious to a person of ordinary skill in the art at the time invention was made to incorporate the solder contacts having diameter less than 100 microns as taught by Svetkoff et al. and the device being bonded to the module

substrate as taught by APA so that interconnect density can be improved and the device size/ground rules can be reduced in Yamamoto and Svetkoff et al's device.

6. Claim 69 is rejected under 35 U.S.C. 103(a) as being unpatentable over Yamamoto (US Pat. 5925931) and Svetkoff et al. (US Pat. 6249347) as applied to claim 40 above, and further in view of Wojnarowski (US Pat. 5888884).

Regarding claim 69, Yamamoto and Svetkoff et al. teach substantially the entire claimed structure as applied to claim 40 above, wherein Yamamoto teach the metal pad comprising three different metals, but Yamamoto and Svetkoff et al. fail to teach the metal pad comprising a stack comprising four different metal levels.

Wojnarowski teaches a device having a pad metallization comprising four or more metal layers/levels comprising an aluminum (40 in Fig. 5-8; Col. 6, line 41), chromium, titanium or nickel-titanium (Col. 7, line 41) and one or more layers/levels of different metals including gold, copper, platinum, etc. (Col. 7, lines 43-46) to provide an improved adhesion and diffusion barrier (Col. 7, lines 36-46).

It would have been obvious to a person of ordinary skill in the art at the time invention was made to incorporate the metal pad comprising a stack comprising four different metal levels as taught by Wojnarowski so that the adhesion, bonding and reliability of metallization can be improved in Yamamoto and Svetkoff et al's device.

7. Claim 70 is rejected under 35 U.S.C. 103(a) as being unpatentable over Yamamoto (US Pat. 5925931), Svetkoff et al. (US Pat. 6249347) and Wojnarowski (US Pat. 5888884) as applied to claims 40 and 69 above, and further in view of Takashi et al. (Japanese Pat. 408236938).

Regarding claim 70, Yamamoto, Svetkoff et al. and Wojnarowski teach substantially the entire claimed structure as applied to claims 40 and 69 above, except the metal stack comprising zirconium as one of the four metals in the stack.

Takashi et al. teach using metal pad/conductor (114 in Fig. 1-4) comprising metals/alloys comprising metal such as zirconium (see abstract in English Translation).

It would have been obvious to a person of ordinary skill in the art at the time invention was made to incorporate the metal stack comprising zirconium as one of the four metals as taught by Takashi et al. so that the desired electrical parameters/properties of the metallization can be achieved and the reliability of the interconnection can be improved Yamamoto, Svetkoff et al. and Wojnarowski's device.

Response to Arguments

8. Applicant's arguments filed on 10-25-04 regarding claims 40, 43-51, 68-72, 74 and 75, have been fully considered, but they are not persuasive as discussed in the previous office action (see examiner's answer dated 08-17-04).

Allowable Subject Matter

9. Claims 76-86 are allowed.

Reasons for Allowance

10. The following is an examiner's statement of reasons for allowance:

The references of record do not teach either singularly or in combination at least the limitations " at least one metal stack formed over said first insulating layer and in contact with said at least one metal layer; a second insulating layer formed over said at least one metal stack" and "an etched solder layer having a thickness of at least 2.33 microns, wherein said etched solder layer forms at least one solder contact in said second insulating layer and in contact with said at least one metal stack" in a semiconductor device having a metal pad layer and first and a second insulating layers.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Nitin Parekh whose telephone number is 571-272-1663. The examiner can normally be reached on 09:00AM-05:30PM.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Eddie Lee can be reached on 571-272-1732. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9318.

Any inquiry of a general nature or relating to the status of this application or proceeding should be directed to the receptionist whose telephone number is 703-308-0956.

NP

12-17-04

NITIN PAREKH

PRIMARY EXAMINER

TECHNOLOGY CENTER 2800